Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) An image printing apparatus that comprises:

a print head for printing images; and

a microcontroller, ~~having~~ in which the processor circuitry is in the form of VLIW processor circuitry, that comprises:

a wafer substrate;

the processor circuitry ~~that is~~ positioned on the wafer substrate;

print head interface circuitry that is positioned on the wafer substrate and is connected between the processor circuitry and the print head, the print head interface circuitry being configured to facilitate communication between the processor circuitry and the print head and to define a number of registers for storing clocking and control information to be received by the print head in accordance with a predetermined algorithm, whereby the print head interface circuitry is connected to a buffer memory that, in turn, is connected to the processor circuitry, the print head interface circuitry being configured to receive a print image from the processor circuitry via the buffer memory in accordance with said clocking and control information and to pass the print image to the print head; and

bus interface circuitry that is discrete from the print head interface circuitry and is connected to the processor circuitry so that the processor circuitry can communicate with devices other than the print head via a bus.

2. (Currently amended) An image printing apparatus that comprises:

a page width print head that is the product of an integrated circuit fabrication technique and which includes a plurality of nozzle arrangements, each nozzle arrangement defining a micro electromechanical device that is capable of being actuated to eject ink from a nozzle chamber of the nozzle arrangement; and

a microcontroller, ~~having~~ in which the processor circuitry is in the form of VLIW processor circuitry, that comprises:

a wafer substrate;

the processor circuitry ~~that is~~ positioned on the wafer substrate;

print head interface circuitry that is positioned on the wafer substrate and is connected between the processor circuitry and the print head, the print head interface circuitry being configured to facilitate communication between the processor circuitry and the print head and to define a number of registers for storing clocking and control information to be received by the print head in accordance with a predetermined algorithm, whereby the print head interface circuitry is connected to a buffer memory that, in turn, is connected to the processor circuitry, the print head interface circuitry being configured to receive a print image from the processor circuitry via the buffer memory in accordance with said clocking and control information and to pass the print image to the print head; and

bus interface circuitry that is discrete from the print head interface circuitry and is connected to the processor circuitry so that the processor circuitry can communicate with devices other than the print head via a bus.

3. (Canceled)

4. (Canceled)

5. (Currently amended) An image printing apparatus as claimed in claim 42, in which the print head interface circuitry is connected to an address and data bus that, in turn, is connected to a central processing unit (CPU) of the microcontroller so that the CPU can address the registers defined by the print head interface circuitry with said clocking and control information.

6. (Canceled)

7. (Currently amended) A microcontroller, in which the processor circuitry is in the form of VLIW processor circuitry, for an image printing apparatus, the microcontroller ~~having VLIW processor circuitry and~~ comprising:

a wafer substrate;

the processor circuitry ~~that is~~ positioned on the wafer substrate;

print head interface circuitry that is positioned on the wafer substrate and is

connected between the processor circuitry and the print head, the print head interface circuitry being configured to facilitate communication between the processor circuitry and the print head and to define a number of registers for storing clocking and control information to be received by the print head in accordance with a predetermined algorithm, whereby the print head interface circuitry is connected to a buffer memory that, in turn, is connected to the processor circuitry, the print head interface circuitry being configured to receive a print image from the processor circuitry via the buffer memory in accordance with said clocking and control information and to pass the print image to the print head; and

bus interface circuitry that is discrete from the print head interface circuitry and is connected to the processor circuitry so that the processor circuitry can communicate with devices other than the print head via a bus.